UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,284	10/22/2003	Manoj Mehrotra	TI-32513.1	4908

23494 7590 03/22/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/691,284	MEHROTRA ET AL.
	Examiner	Art Unit
	DiLinh Nguyen	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9, 11-17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsui (U.S. Pat. 5792699) (previously applied) in view of Fulford, Jr. et al. (U.S. Pat. 5898202) (previously applied).

- Regarding claims 9, 15 and 17, Tsui discloses a transistor comprising:

a gate structure outwardly of a semiconductor substrate 1, wherein the gate structure comprises a gate 6, a gate insulator 5;

a source region and a drain region 8 in the substrate 1, wherein the source region and the drain region are formed using the gate structure as a mask, wherein the source region and the drain region each define a bottom junction at bottom portions thereof and a sidewall junction at sidewall portions thereof between the respective source and drain region and the substrate;

a channel 4 defined in the substrate inwardly of the gate structure and between the source and drain regions; and

a bottomwall/sidewall junction capacitance reduction region 4 (fig. 2c) and 4+9 (cover fig.) extending within and between the source region and the drain region, wherein the bottomwall/sidewall junction capacitance reduction region

extends at least partially through the bottomwall junction and the sidewall junction of the source region and the drain region (cover fig., column 5, lines 53-60 and abstract), and

wherein the dopant concentration of the bottomwall/sidewall junction capacitance reduction peaks substantially at the bottomwall junction (figs. 2b-2c, column 2, lines 45-52).

Tsui does not disclose sidewalls.

However, Fulford, Jr. et al. disclose a transistor comprising:

a gate structure outwardly of a semiconductor substrate, wherein the gate structure comprises a gate 606, a gate insulator 604 and sidewalls 614b (cover fig., column 23, lines 20-25). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Tsui by having a sidewalls because as taught by Fulford, Jr. et al., in order to protect the gate structure and optimize silicon area reduction (cover fig. and abstract).

- Regarding claim 11, Tsui discloses that the transistor is an n-MOS type transistor (column 5, line 9) and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 50-200 kev (column 5, lines 54-55).
- Regarding claim 12, Tsui discloses that the transistor is a p-MOS type transistor (column 5, lines 9) and the bottomwall/sidewall junction capacitance reduction region is implanted using energies of about 50-200 kev (column 5, lines 54-55).

Moreover, the implantation using energies would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed the implantation using energies of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen the energies or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed, Cir. 1990).

- Regarding claim 13, Tsui and Fulford disclose that a non-encroachment distance (the shortest distance between the base of the gate) would be at least about 150 angstroms (cover fig.).
- Regarding claims 14 and 19, Tsui discloses that at least a portion of the bottomwall/sidewall junction capacitance reduction region is implanted through the gate structure (cover fig.).
- Regarding claim 20, Tsui discloses that a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaks substantially at the bottomwall junction (figs. 2b-2c, column 2, lines 45-52).
- Regarding claim 16, Tsui discloses that the bottomwall/sidewall junction capacitance reduction region is formed with the same mask configuration as is used during the formation of the source and drain regions (cover fig.).

3. Claims 10 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsui (U.S. Pat. 5792699) (previously applied) in view of Fulford, Jr. et al. (U.S. Pat. 5898202) (previously applied) and further in view of Baliga (U.S. Pat. 6781194) (previously applied).

Tsui and Fulford, Jr. et al. substantially disclose all the limitations as claimed above except for a concentration of dopants implanted to form the bottomwall/sidewall junction capacitance reduction region is about $1x10^{12}$ cm^{-2} to $1x10^{14}$ cm^{-2}.

However, Baliga disclose a semiconductor device comprising a concentration of dopants implanted to form a junction region is about $1x10^{12}$ cm^{-2} to $7x10^{12}$ cm^{-2} (abstract). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Tsui by having a concentration of dopants implanted to form a junction region is about $1x10^{12}$ cm^{-2} to $7x10^{12}$ cm^{-2}, as taught by Baliga, in order to enhance forward on-state and reverse breakdown voltage characteristics for the semiconductor device (abstract).

Moreover, the concentration of dopants would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed the concentration of dopants of any unexpected results arising therefrom. Where patentability is aid to be

based upon particular chosen concentration of dopants or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed, Cir. 1990).

Response to Arguments

Applicant's arguments filed 1/9/06 have been fully considered but they are not persuasive.

- The applicant argues that Tsui does not disclose a bottomwall/sidewall capacitance reduction region extending within and between the source and drain region that extends partially through the bottomwall junction thereof.

The arguments have been fully considered but they are not persuasive because Tsui clearly discloses region 4 (fig. 2c), regions 4 and 9 (cover fig. and abstract) function as the bottomwall/sidewall capacitance reduction region extending within and between the source and drain region that extends partially through the bottomwall junction thereof (region 9, cover fig.); wherein the source and drain regions each define a bottomwall junction at bottom portions of the source and drain regions (cover fig.).

- The applicant argues that the combination of Tsui and Fulford, Jr. et al. do not disclose teach or suggest a dopant concentration of the bottomwall/sidewall junction capacitance reduction region peaking substantially at the bottomwall junction.

The arguments have been fully considered but they are not persuasive

because Tsui discloses that the dopant concentration of the bottomwall/sidewall junction capacitance reduction peaks substantially at region 4; wherein a portion of region 4 is extending under the bottom portions (bottomwall junction) of the source and drain 8 (figs. 2b-2c, column 2, lines 45-52).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN

HOA PHAM
PRIMARY EXAMINER